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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/881,408	06/13/2001	Kie Y. Ahn	MI22-1534	8492
21567	7590	04/18/2005	EXAMINER	
WELLS ST. JOHN P.S. 601 W. FIRST AVENUE, SUITE 1300 SPOKANE, WA 99201			LE, THAO X	
			ART UNIT	PAPER NUMBER
			2814	

DATE MAILED: 04/18/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

09/881,408

Applicant(s)

AHN ET AL.

Examiner

Thao X. Le

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 14 July 2004.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-19, 52, 56-58 and 60-62 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 3-5, 56-58 and 62 is/are allowed.
- 6) ☒ Claim(s) 1, 2, 6, 7, 16, 17, 52, and 60-61 is/are rejected.
- 7) ☒ Claim(s) 8-15 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 06/13/01 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |   |   |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)   | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)  | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date <u>23 Dec. 2004</u> . | 6) <input type="checkbox"/> Other: _____  |

## DETAILED ACTION

1. Claims 20-31, 54-55 and 59 are cancelled in the amendment dated 28 Feb. 2005

### ***Claim Rejections - 35 USC § 102***

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1, 2, 6-7, 19, 52, 60-61 are rejected under 35 U.S.C. 102(e) as being anticipated by US 6679996 to Yao et al.

Regarding claim 1, Yao discloses a method of forming a dielectric layer in fig. 1A-2C comprising: a semiconductor substrate 1, fig. 1A, having a silicon-containing surface, column 3 line 57, forming a first metal-containing dielectric layer 3'B consisting of metal oxide, column 4 line 22, over the surface, all the metal of the first dielectric layer 3'B consisting of at least one element selected from Group IVB of the Periodic Table, column 4 line 22, and forming a second metal-containing dielectric layer 3'A of metal oxide on and in contact with the first metal-containing dielectric layer 3'B, fig. 2C, all the metal of the second dielectric layer 3'A consisting of at least one element selected from Group IIIB of the Periodic Table, column 4 line 32, including the first and

second metal-containing dielectric layers 3'A/3'B in an integrated circuit device (semiconductor device, a transistor, a memory, etc.). Yao discloses the metal oxide layer can be used in the integrated circuit device such as semiconductor device, a transistor, a memory, etc., column lines 15-19.

A recitation of 'the first and second metal-containing dielectric layers 3'A/3'B in an integrated circuit device' of the claimed invention does not result in a structural difference between the claimed invention and the prior art, thus claimed invention is only an art recognized suitability for an intended purpose, MPEP 2144.07.

Regarding claims 2, 6-7, 60-61, Yao discloses the method wherein the metal of the first metal-containing dielectric layer 3'B consists of hafnium, column 4 line 22, wherein the metal of the second metal-containing dielectric layer 3'A consists of one element selected from Group IIIB of the periodic table, wherein the second metal-containing dielectric layer 3 consists of lanthanum, column 4 line 32.

Regarding claim 19, Yao discloses the method wherein the first metal-containing dielectric layer 3'B, fig. 2C, consists of hafnium oxide, column 4 line 22, and the second metal-containing dielectric layer 3'B, fig. 2C, consists of lanthanum oxide, column 4 line 32.

Regarding claim 52, Yao discloses a method of forming a dielectric layer in fig. 1A-2C comprising: providing a semiconductor substrate 1, fig. 1A, comprising a silicon-containing surface, column 3 line 57, forming a first metal-containing dielectric layer 3'B over the surface, fig. 2C, the first dielectric layer 3'B consisting essentially of hafnium

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oxide, column 4 line 22, forming a second metal-containing dielectric layer 3'A on and in contact with the first metal-containing dielectric layer 3'B, fig. 2C, the second dielectric layer consisting essentially of lanthanum oxide, column 4 line 32, and including the first and second metal-containing dielectric layers 3'A/3'B in an integrated circuit device (semiconductor device, a transistor, a memory, etc.). Yao discloses the metal oxide layer can be used in the integrated circuit device such as semiconductor device, a transistor, a memory, etc., column lines 15-19.

A recitation of 'the first and second metal-containing dielectric layers 3'A/3'B in an integrated circuit device' of the claimed invention does not result in a structural difference between the claimed invention and the prior art, thus the claimed invention is only an art recognized suitability for an intended purpose. MPEP 2144.07.

### ***Claim Rejections - 35 USC § 103***

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation

under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

6. Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over US 6679996 to Yao et al.

Regarding claim 18, Yao does not disclose the method wherein forming the first metal-containing dielectric layer and second dielectric containing layer comprises forming the layers to have respective thickness having ratio of from about 4:1 to about 1:4.

However, Yao discloses the metal oxide layer 3'A and 3'B having a thickness about 0.001 and 10  $\mu\text{m}$ , column 10 lines 31. Accordingly, it would have been obvious to one of ordinary skill in art to use thickness teaching of Yao in the range as claimed, because it has been held that where the general conditions of the claims are disclosed in the prior art, it is not inventive to discover the optimum or workable range by routine experimentation. See *In re Aller*, 220 F.2d 454, 105 USPQ 233, 235 (CCPA 1955).

7. Claims 1 and 16-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over US 6784508 to Tsunashima et al. in view of US 6573197 to Callegari et al.

Regarding claim 1, Tsushima discloses a method of forming a dielectric layer in fig. 2G-3 comprising: a semiconductor substrate 1, fig. 2G, having a silicon-containing surface, forming a first metal-containing dielectric layer 6 comprising of metal silicate

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(metal silicon-oxygen material), column 5 line 26, over the surface, the metal of the first dielectric layer consisting of at least one element selected from Group IVB of the periodic table, column 5 line 26, and forming a second metal-containing dielectric layer 3 of metal oxide on and in contact with the first metal-containing dielectric layer 6, all the metal of the second dielectric layer 3 consisting of at least one element selected from Group IIIB of the periodic table, column 5 line 35, and including the first and second metal-containing dielectric layers 6/3 in an integrated circuit device, fig. 1A.

However, Tsunashima does not disclose the first metal-containing dielectric layer 6 consisting of metal oxide.

However, Callegari discloses the method of forming a dielectric layer in fig. 2-4 comprising providing a substrate 10 comprising silicon-containing surface, column 3 line 62, forming a first metal-containing dielectric layer 14 consisting of metal oxide, and all the metal of the first dielectric layer consisting of at least one element selected from Group IVB of the periodic table column 4 lines 57 or metal silicate, column 4 line 57. At the time of the invention was made; it would have been obvious to one of ordinary skill in the art to use the dielectric layer 14 teaching of Callegari to replace the layer 6 of Tsunashima, because such material substitution would have been considered a mere substitution of art-recognized equivalent values in creating a high k-dielectric material, MPEP 2144.06

Regarding claims 16-17, Tsushima discloses a method wherein forming the hafnium-containing layer and the lanthanum-containing layer comprises LPCVD, column 6 line 47, CVD or the like, column 11 line 66.

But, Tsushima does not disclose the method comprises physical vapor deposition or electron beam evaporation.

However, Callegari discloses the method wherein the metal oxide layer can be deposited by different method such as CVD, PVD (sputtering), electron beam evaporation in column 5 lines 13-18. At the time the invention was made; it would have been obvious to one of ordinary skill in the art to use the method of depositing metal oxide teaching of Callegari in Tsushima's method, because such method of depositing metal oxide is conventional as taught by Callegari, column 5 lines 13-15.

#### ***Allowable Subject Matter***

8. Claims 3-5 and 62 are allowed because the prior art of record neither anticipated nor rendered obvious all the limitations of the base claim 3 including heating the metal layer and layer of silicon dioxide to a temperature of from about 200<sup>0</sup>C to less than 400<sup>0</sup>C and combining metal of the metal layer with oxygen of the silicon dioxide layer to form a metal oxide dielectric material comprised by a first metal containing dielectric layer over the substrate, all the metal of me first dielectric layer consisting of at least one element selected from Group IVB of the periodic table; and forming a second metal-containing dielectric layer on and in contact with the first metal-containing dielectric

layer, all the metal of the second dielectric layer consisting of at least one element selected from Group IIIB of the periodic table.

9. Claims 8-15 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. The prior art of record neither anticipated nor rendered obvious the limitation 'exposing the hafnium-containing layer and the lanthanum-containing layer to an oxygen comprising atmosphere and heating the hafnium-containing layer and the lanthanum-containing layer to a temperature effective to form a hafnium-containing dielectric layer and a lanthanum-containing dielectric layer'.

10. Claims 56-57 are allowed because the prior art of record neither anticipated nor rendered obvious all the limitations of the base claim 56 including exposing the hafnium-containing layer and the lanthanum layer to an oxygen comprising atmosphere by ion bombardment using an ion bombardment energy of about 10 electron volts (eV) or less, and heating the hafnium-containing layer and the lanthanum layer to a temperature effective to form a hafnium-containing dielectric layer and a lanthanum-containing dielectric layer.

11. Claim 58 is allowed because the prior art of record neither anticipated nor rendered obvious all the limitations of the base claim 58 including forming a layer of silicon dioxide overlying at least one portion of the surface; forming a hafnium-containing layer over the layer of silicon dioxide; combining hafnium of the hafnium-containing layer with oxygen of the silicon dioxide layer to form a hafnium oxide over the

surface; forming a lanthanum-containing layer over the hafnium-containing layer and positioning the substrate within a reaction chamber and exposing the hafnium-containing layer and the lanthanum-containing layer to oxygen radicals within the reaction chamber and heating the hafnium-containing layer and the lanthanum-containing layer to a temperature effective to form a hafnium-containing dielectric layer and a lanthanum-containing dielectric layer.

### ***Conclusion***

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thao X. Le whose telephone number is (571) 272-1708. The examiner can normally be reached on M-F from 8:00 AM - 4:30 PM.

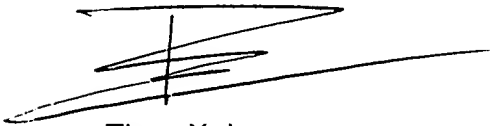
If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael M. Fahmy can be reached on (571) 272 -1705. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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Thao X. Le  
Patent Examiner  
12 April 2005